# MULTIPLE DEVICE SUPPORT FOR THE Si3034/35/44/56

## 1. Introduction

A key feature of the Si3035 (FCC/Japan), Si3034/44 (global), and Si3056 (global) direct access arrangement chipsets is their ability to be cascaded on a common serial interface. This type of circuit is commonly referred to as a master/slave configuration. The master/slave capability of these DAA products is accomplished by programming the system-side device (either the Si3021 or Si3056) as described in this document.

The Si3021 or Si3056 system-side devices provide the support for this multiple device operation on a common serial interface. Generally, an Si3021 or Si3056 is used as a master to control up to seven additional devices on a single serial interface. The Si3021 or Si3056 system-side device can also be slaved to an ASIC. With an ASIC as the master, there can be up to eight slaved DAA chipsets sharing a common serial interface.

### 1.1. Si3021/56 Master with Single Slave

A common application for Silicon Labs serial interface DAAs (Si3034/35/44/56) is to be used with the Si3000 (voice codec) in applications such as a data/fax/voice modem (Figure 1 on page 3 and Figure 2 on page 4). In this configuration, the Si3021/56 (master) will be set in serial mode 0 or 1 (Table 1). The Si3000 should be configured as a slave. On power up, the Si3021/56 master device will be unaware of the additional device on the serial bus. The FC/$\overline{\text{RGDT}}$ pin is an input operating as the hardware control for secondary frames. The $\overline{\text{RGDT}}$/FSD pin is an output operating as the active low ring detection signal. The master device should be programmed for master/slave mode prior to enabling the patented capacitive communications link to prevent a ring signal from falsely transitioning the slave device's FSYNC input.

**Table 1. Serial Modes**

| Mode | M1 M0 | Description |
|---|---|---|
| 0 | 0 0 | $\overline{\text{FSYNC}}$ frames data |
| 1 | 0 1 | $\overline{\text{FSYNC}}$ pulse starts data frame |
| 2 | 1 0 | Slave mode |
| 3 | 1 1 | Reserved |

The first step to enabling multiple devices is the programming of the MCLK rate and the sample rate of the master. When using multiple devices, the sample rate should remain fixed. Varying the sample rate will cause the PLLs in the slave devices to lose lock and require time to re-synchronize. During this time the behavior of the parts will be unpredictable. To program the MCLK and sample rate, refer to the "Clock Generation Subsystem" section of the appropriate DAA data sheet. The SCLK generated by the master device is fed into the MCLK of the slave. When the Si3021 is in slave mode (serial mode 2), the internal PLLs are set to a fixed multiply by 20. The Si3056 will set M1 and N1 based on the following equation:

$$256 \times \text{sampling rate} \times \frac{M1}{N1} = 98.304\ \text{MHz}$$

This will ensure an identical sample rate for each device.

Register 14 provides the necessary control bits to configure the Si3034/35/44/56 for master/slave operation. When the Si3021/56 is in serial mode 0 or 1 (master), the default value of Register 14 is 02h for the Si3021 and 00h for the Si3056. When the Si3021/56 is in serial mode 2 (slave), the default value is 3Fh for the Si3021 and 3Dh for the Si3056. This register should be programmed after the PLLs are programmed and before enabling the capacitive communication link.

The three most significant bits of Register 14 (NSLV[2:0]) set the number of slave devices to be supported on the serial bus. For each slave, the Si3021/56 configured as the master will generate a $\overline{\text{FSYNC}}$ to the DSP.

The next two bits of Register 14 (SSEL[1:0]) determine the type of signaling used in the LSB of SDO. This can assist the DSP in isolating which data stream is the master and which is the slave. The default SSEL for the slave device will be 11b, indicating 15-bits of SDO receive data stream with the LSB = 0. If a 16-bit data stream is desired, the SSEL must be set to 00b.

Bit 2 of Register 14 is the delayed frame sync control (FSD) bit. This will select the number of SCLKs from the beginning of the primary frame (output on $\overline{\text{FSYNC}}$) to the generation of the delayed frame sync (FSD) signal from the master. If the FSD bit is high, the FSD signal will be generated 16 SCLKs after the beginning of the primary frame. In this mode, the slave device will be signaled to send or receive data immediately after the master finishes sending or receiving the 16-bit stream

(see Figure 3 on page 5). This is the recommended setting when using a Si3021/56 as the master and using either the Si3021/56 or the Si3000 as a slave.

If the FSD bit is set low, the FSD signal will be generated 32 SCLKs after the start of the primary frame. This will allow 16 SCLKs after the data transfer of the master before the data transfer occurs for the slave (see Figure 4 on page 5). If the master is using serial mode 0 (where the FSYNC frames the data), it is necessary to have 32 SCLKs. This will allow the FSYNC signal to go high before pulsing low to frame the data for the slave (see Figure 5 on page 5). This mode is not recommended for Silicon Laboratories devices and is only mentioned as a possible solution when using a non-Silicon Laboratories codec as the slave.

In daisy-chain mode (DCE=1), the polarity of the ring signal can be controlled by bit 1 (RPOL) of Register 14. When RPOL =1, the ring detect signal is active high. Bit 0, Daisy Chain Enable (DCE), sets the Si3021/56 in master/slave mode. When this bit is set, the FC/RGDT pin becomes the ring detect output and the RGDT/FSD pin becomes the delay frame sync output.

Once the control registers of the master have been programmed, the communications link of each device can be enabled. It is up to the DSP or ASIC controlling the devices to track the time frames to ensure data is being transferred to and from the intended device.

## 1.2. Si3021/56 Master with Multiple Slaves

The Si3021/56 can support up to seven slave devices on a single serial bus. The master must be set in serial mode 1. The slave devices must be in serial mode 2 (see Figure 6 on page 6 and Figure 7 on page 7). The PLLs of the master device should be configured on start up. The number of slaves is set with the NSLV[2:0] bits of Register 14 in the master Si3021/56 and the FSD bit should be set high. These settings are used to avoid bus contention and false signaling. Figure on page 8 shows the relative timing for one master and three slave devices. After the master has been appropriately programmed, the communication between the line-side and system-side devices in the DAA chipset can be enabled on each of the slaves.

## 1.3. ASIC Master with single Si3021/56 Slave

In certain cases it may be desired to have the Si3021/56 in slave mode without a Si3021/56 as the master (see Figure 9 on page 9 and Figure 10 on page 10). This can be done if the proper signals are sent from the ASIC to the Si3021/56.

The most important concern is the clock rate. When in serial mode 2, the Si3021 internal PLLs are set to a fixed multiply by 20 to generate the sample rate.

The Si3056 will set M1 and N1 based on the following equation:

$$256 \times \text{sampling rate} \times \frac{M1}{N1} = 98.304\ \text{MHz}$$

The ASIC must supply a clock signal to MCLK that equals 256*Fs, where Fs is the desired sample rate. This clock signal should have less than 100 ppm edge-to-edge jitter. During normal operation in this configuration, the clock signal should not be changed. On startup, the Si3021/56 should be held in reset until the MCLK input is stable. After RESET transitions high, SDI should remain 0 for a minimum of 1 msec to allow the PLLs to lock.

Another signal of concern is the frame sync signal (FSYNC). This would normally be the FSD signal coming from the master. In serial mode 2, the Si3021/56 expects an FSYNC input from the master that frames the serial data. When using an ASIC as the master, the ASIC must generate this FSYNC for the Si3021/56 (see Figure 9 on page 9 and Figure 10 on page 10).

## 1.4. ASIC Master with multiple Si3021/56 Slave

Using the same signaling scheme, up to eight system-side devices (either eight Si3021s or eight Si3056s) may share the same serial interface (see Figure 12 on page 11). In this case, the clocking procedures used in the previous situation still apply. The ASIC will generate the FSYNC for the first slave, then each slave will generate an FSD output which will be the FSYNC input for the next slave in the chain. It is imperative that the ASIC keeps track of time slots and which slave is handling data in which time slot (see Figure 13 on page 12 and Figure 14 on page 13).

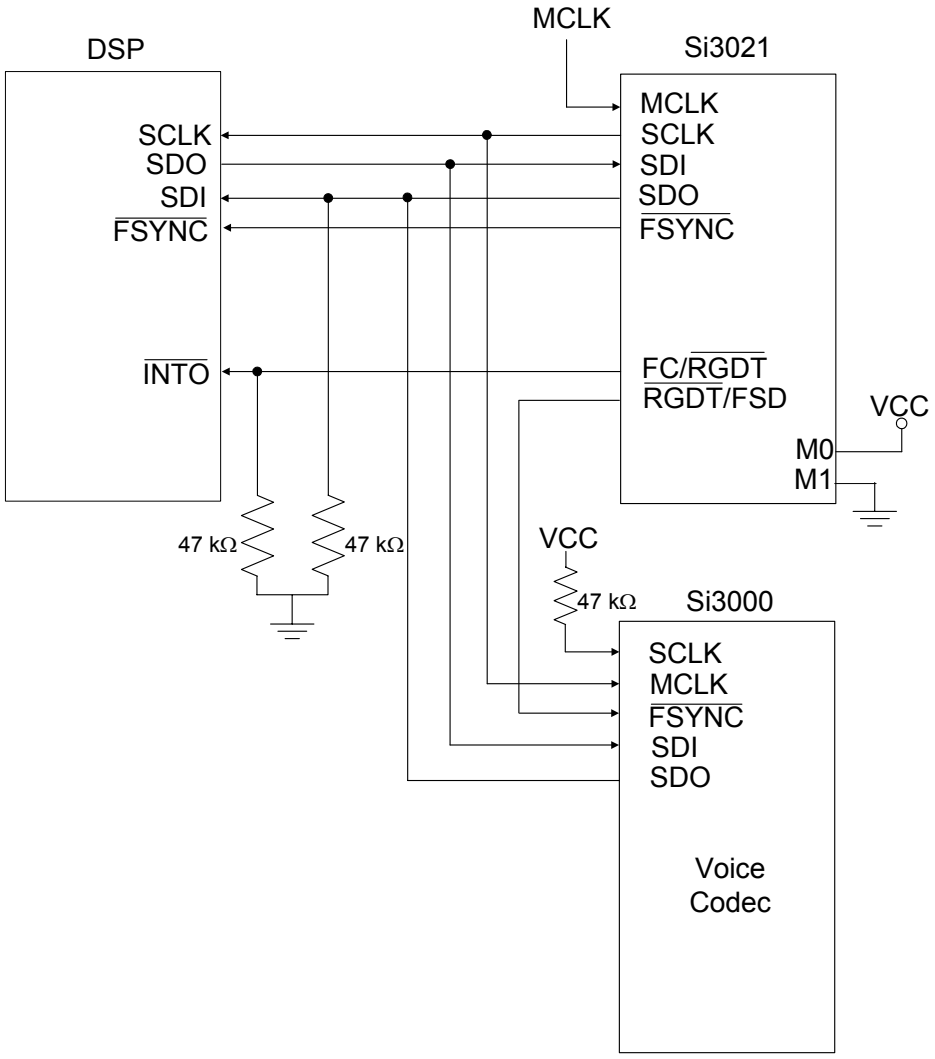


**Figure 1. Si3021 Typical Connection for Master/Slave Operation (e.g., Data/Fax/Voice Modem)**

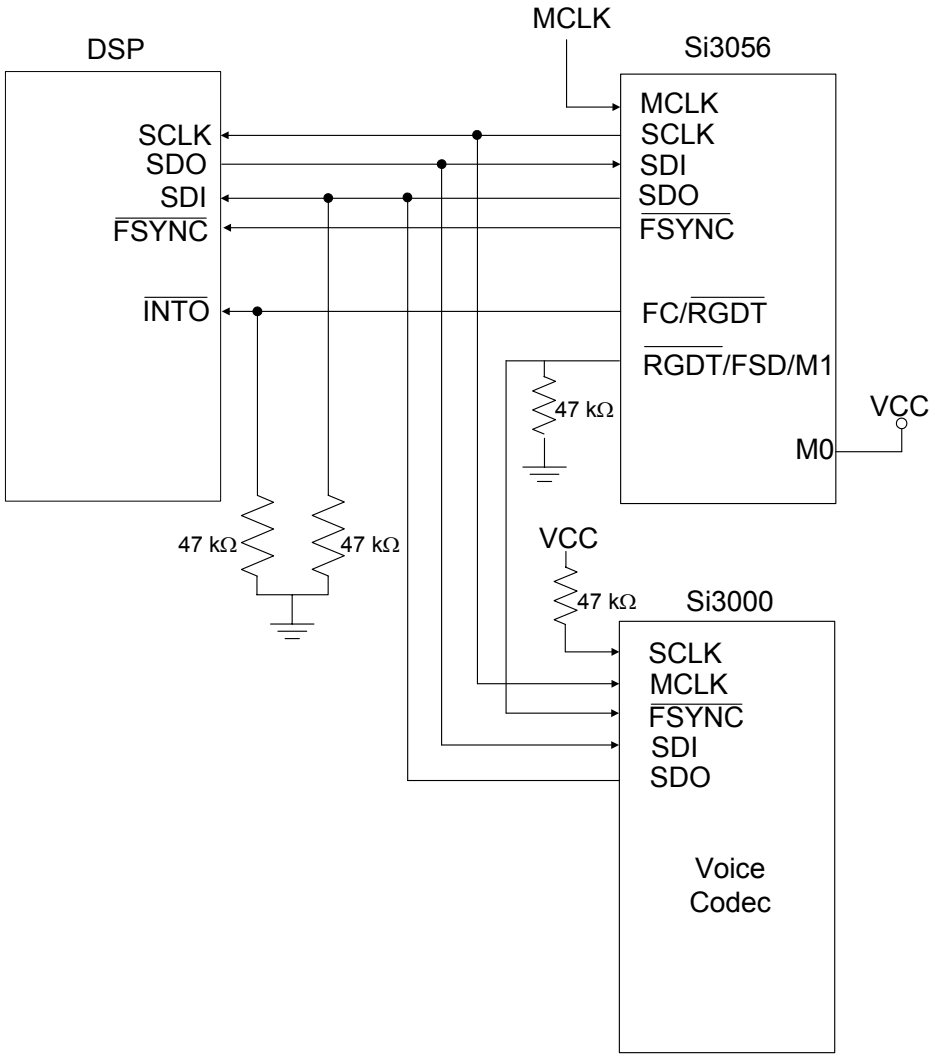


**Figure 2. Si3056 Typical Connection for Master/Slave Operation (e.g., Data/Fax/Voice Modem)**

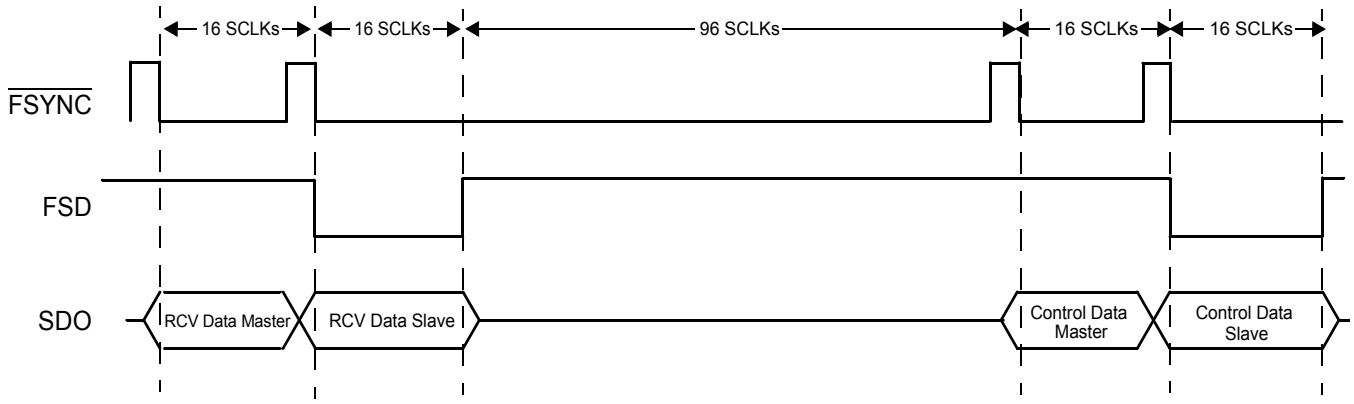


**Figure 3. One Master, One Slave, Master Serial Mode 1, FSD Bit 1**

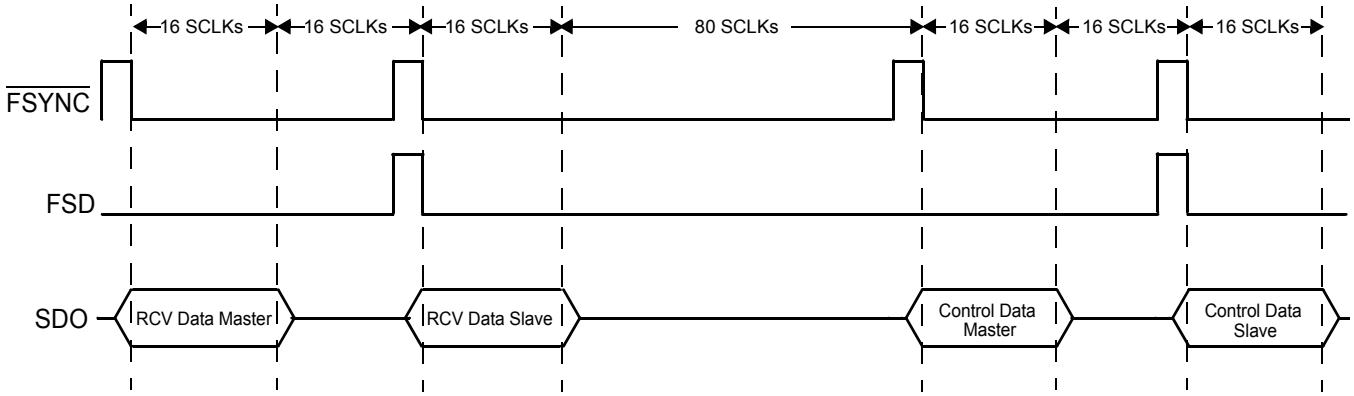


**Figure 4. One Master, One Slave, Master Serial Mode 1, FSD Bit 0**

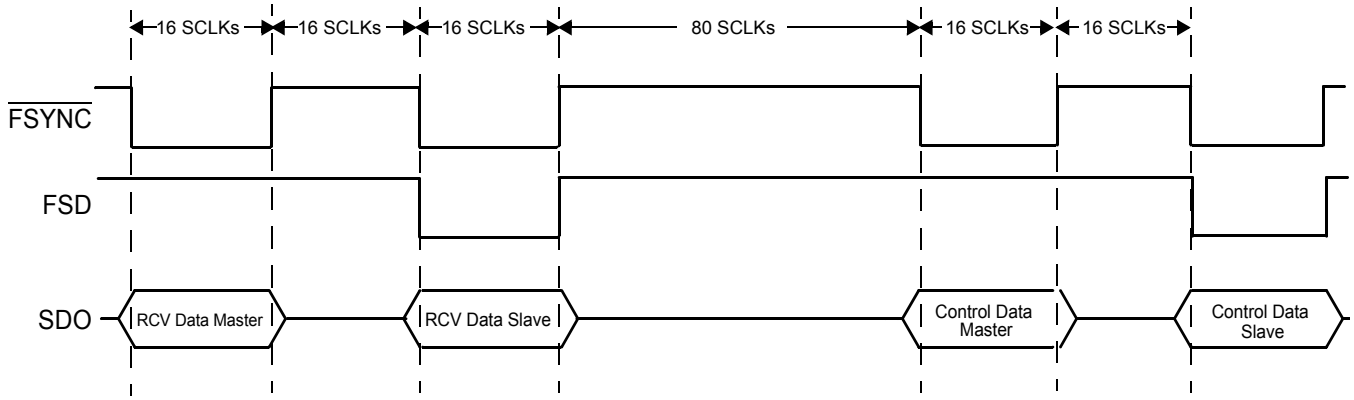


**Figure 5. One Master, One Slave, Master Serial Mode 0, FSD Bit 0**

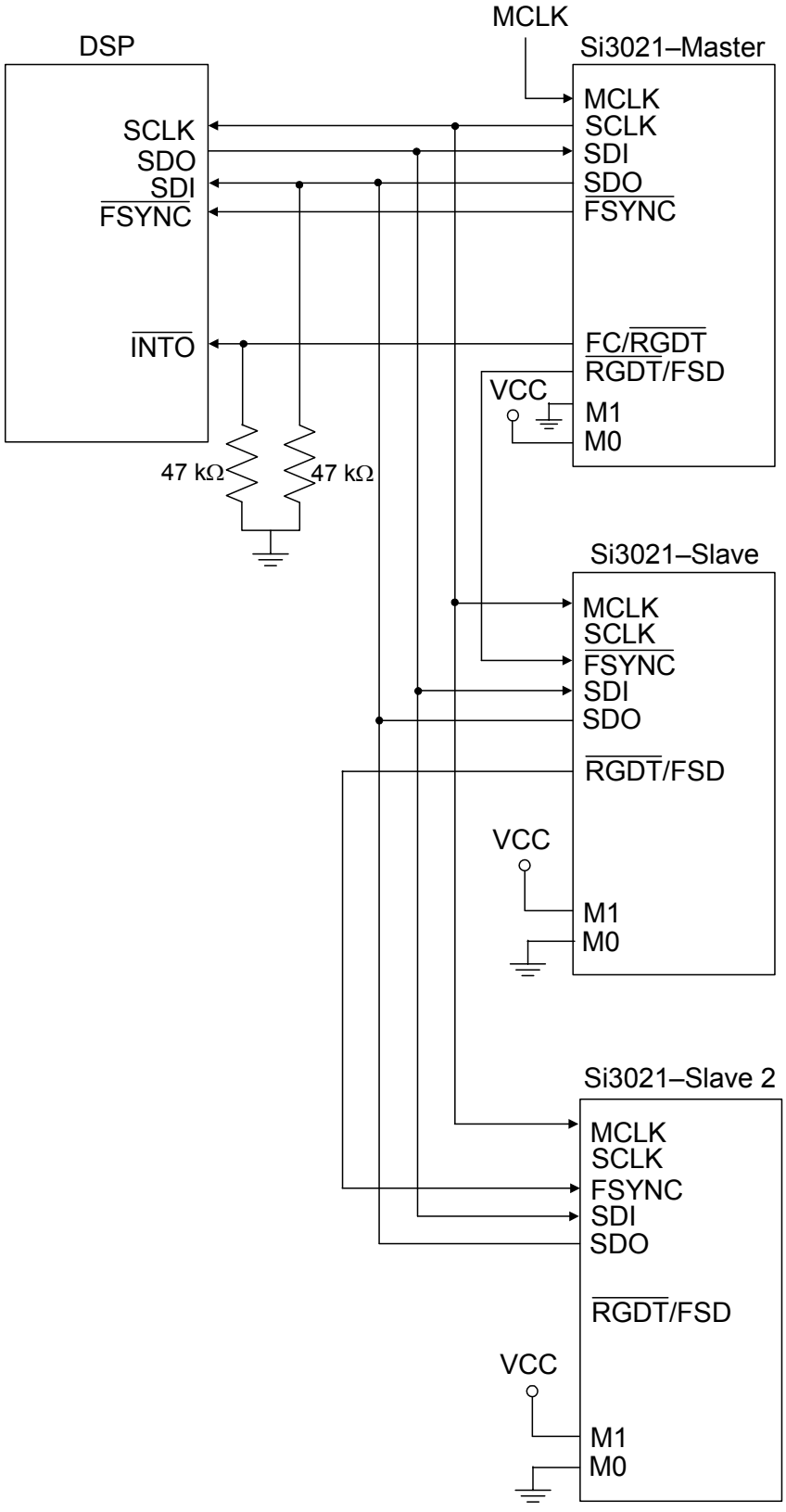


**Figure 6. Typical Connection for Multiple Si3021s**

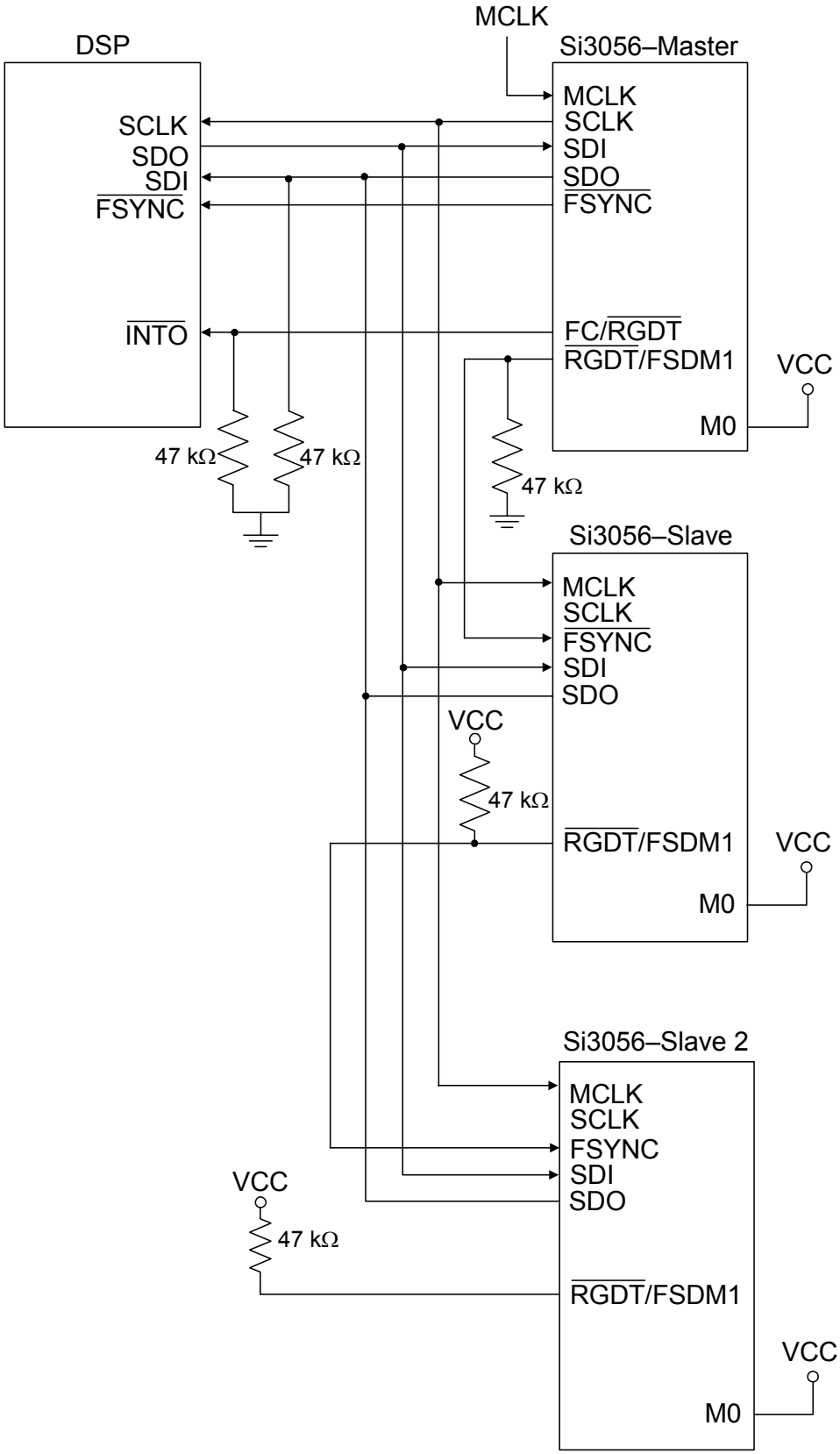


**Figure 7. Typical Connection for Multiple Si3056s**

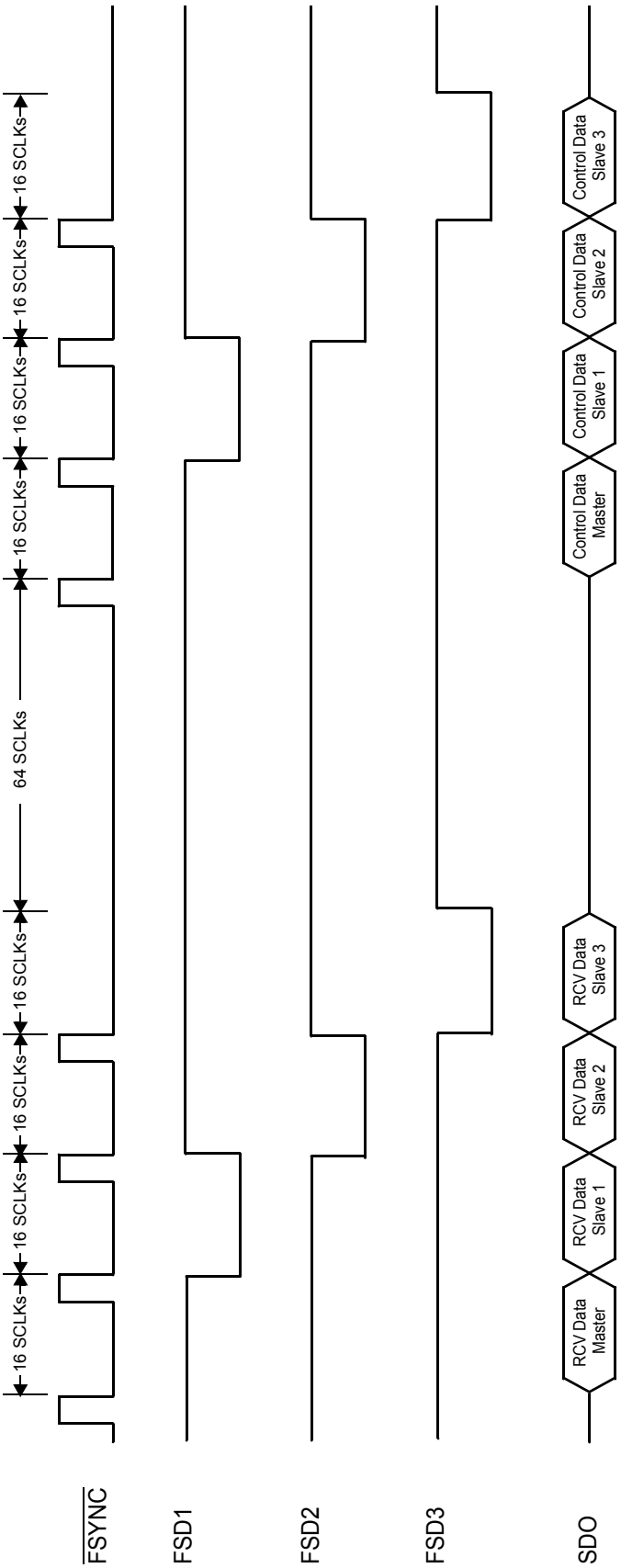


**Figure 8. One Master, Three Slaves, Master Serial Mode 1, FSD = 1**

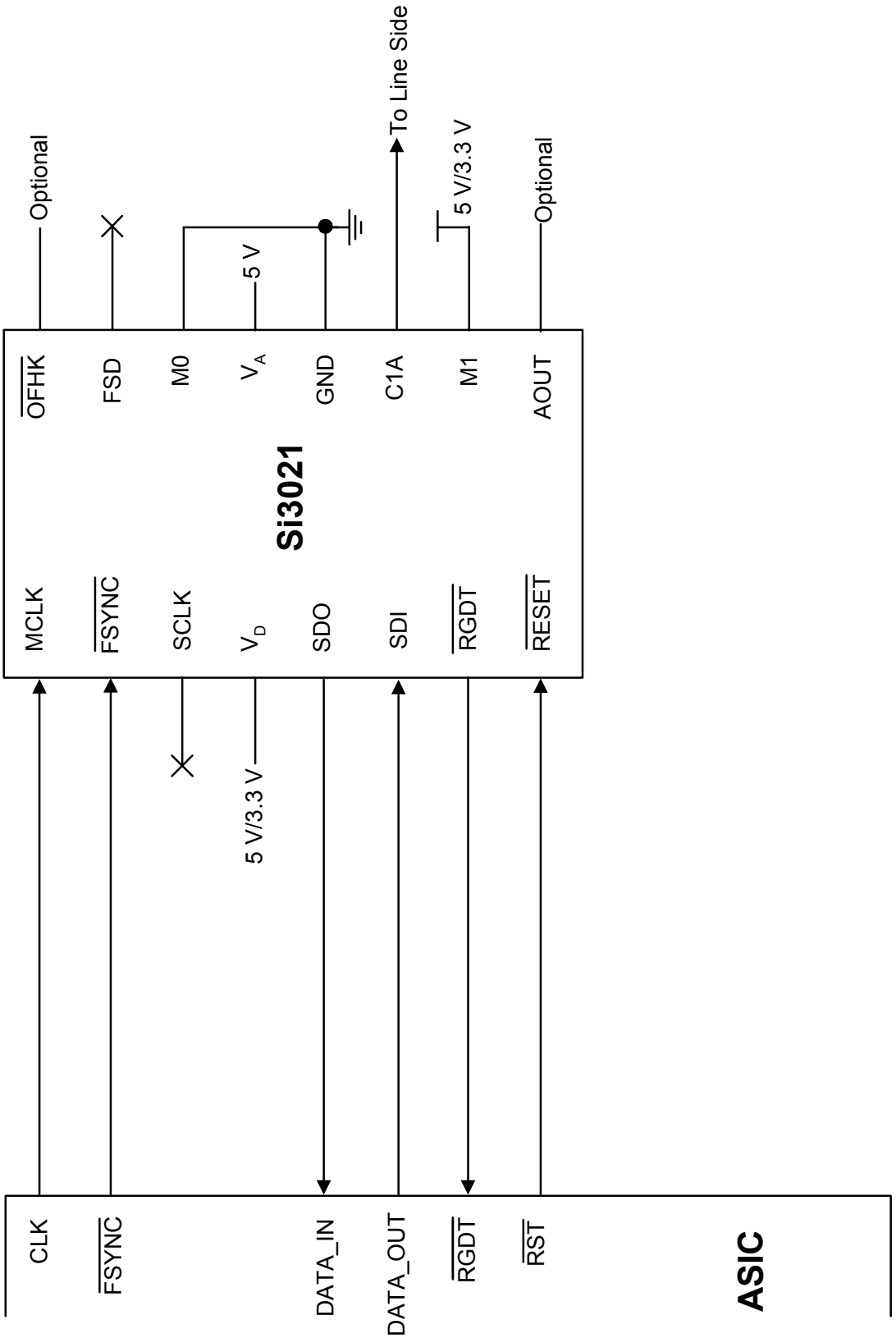


**Figure 9. Si3021 as Single Slave to ASIC**

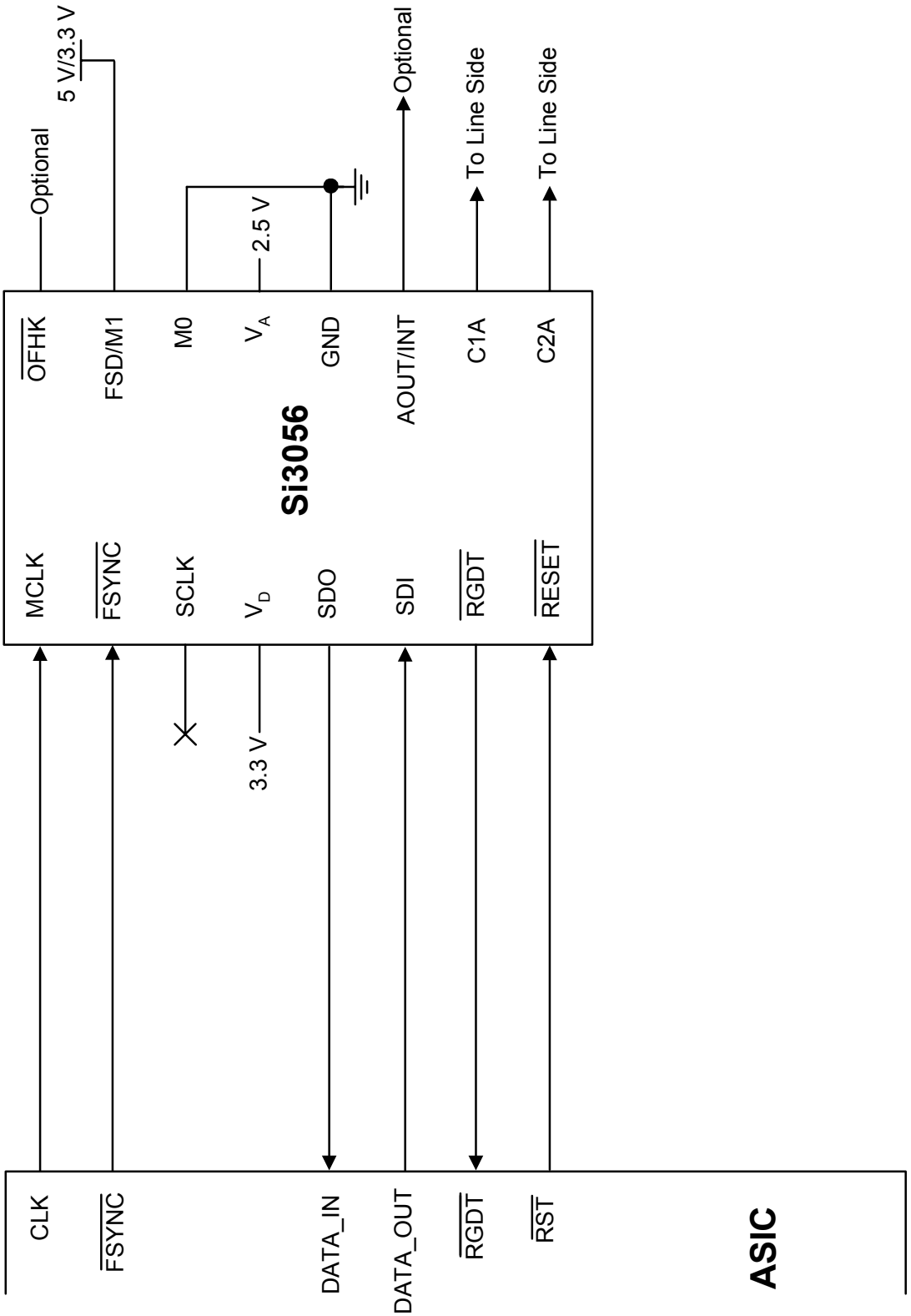


**Figure 10. Si3056 as Single Slave to ASIC**

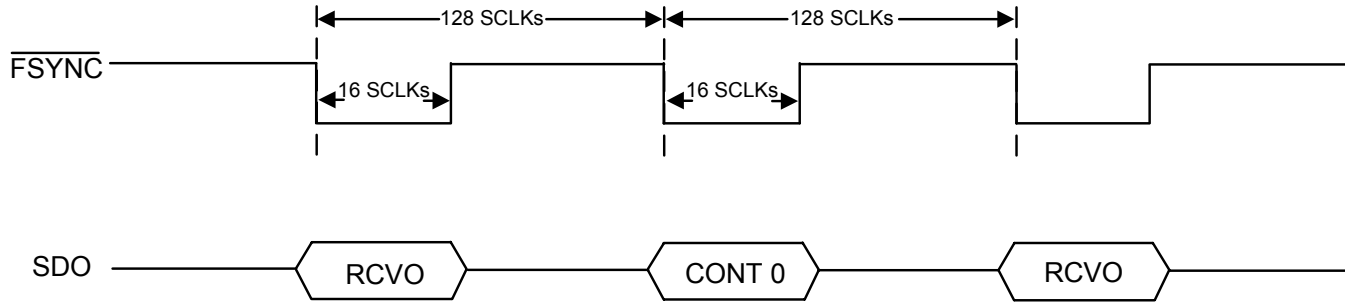


**Figure 11. Relative Timing, Single Slave, ASIC Master**

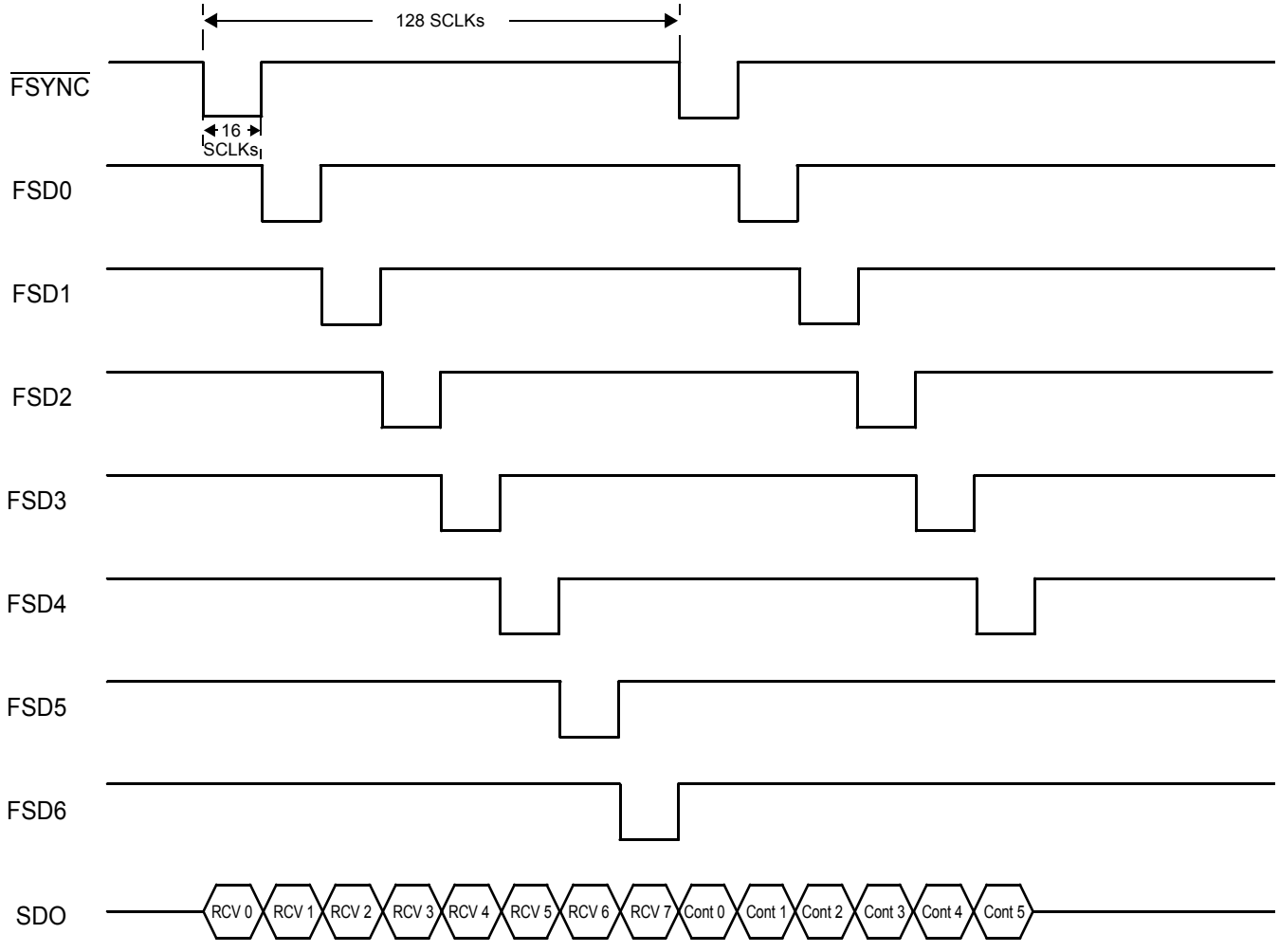


**Figure 12. Relative Timing, Multiple Slaves, ASIC Master**

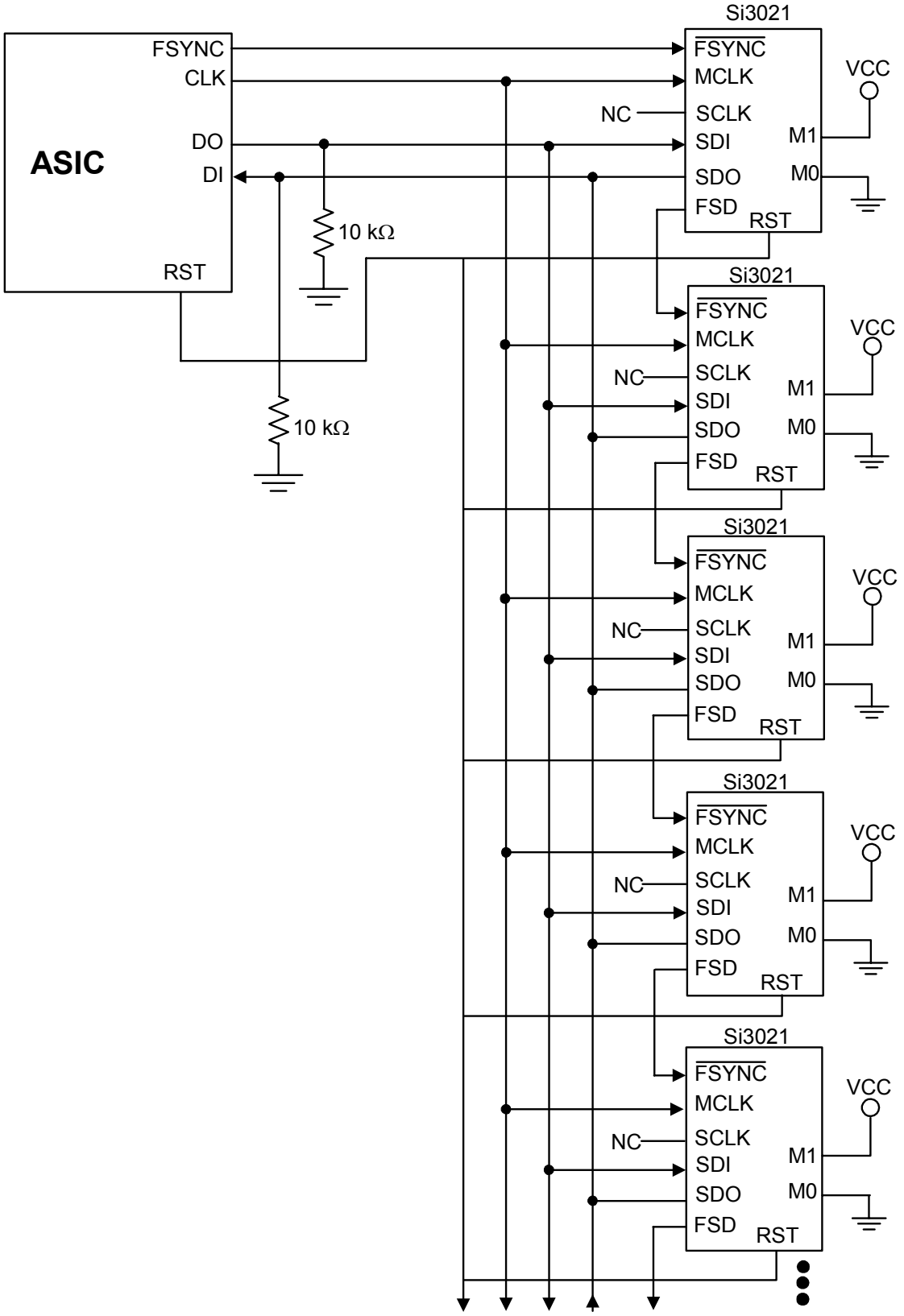


**Figure 13. Typical Connection of Multiple Si3021s as Slaves, ASIC Master**

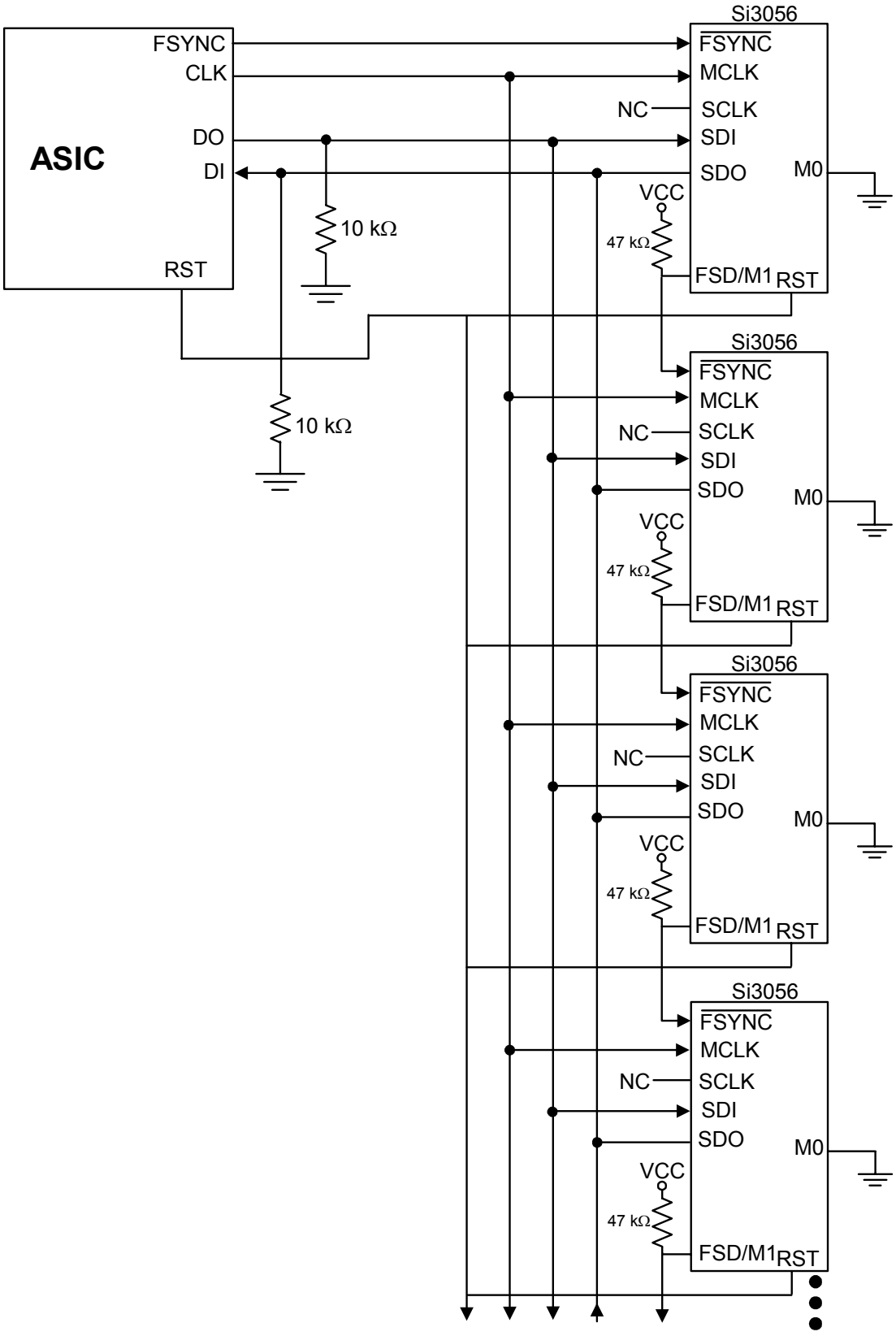


**Figure 14. Typical Connection of Multiple Si3056s as Slaves, ASIC Master**

# DOCUMENT CHANGE LIST

## Revision 0.2 to Revision 0.3

- Added Si3056 daisy-chain support description.

## NOTES:

## CONTACT INFORMATION

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